AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A process for producing a reflection type liquid crystal display device, comprising the steps of:

(a) depositing a low resistance metal layer on an insulating substrate, and using a first mask to pattern the metal layer to form [[a]] source/drain ~~wiring by using a first mask~~ electrodes;

(b) depositing a silicon layer, gate insulating film and gate electrode layer on said insulating substrate having said source/drain ~~wiring pattern~~ electrodes formed thereon in this order, and using a second mask to pattern the silicon layer, the gate insulating film and the gate electrode layer to form a thin film transistor region and a gate ~~wiring by using a second mask~~ electrode;

(c) depositing a passivation film on said insulating substrate having said source/drain ~~wiring~~ electrodes, said thin film transistor region and said gate ~~wiring~~ electrode formed thereon, and using a third mask to form [[an]] a first opening ~~for~~

~~the transistor~~ through said passivation film ~~at a predetermined position on~~ to said source electrode ~~wiring by using a third mask~~;

(d) depositing an interlayer insulating film on said passivation film, forming a rough surface of said interlayer insulating film, and using a fourth mask to form [[an]] a second opening ~~for the transistor~~ through said interlayer insulating film at a position corresponding to the first opening ~~formed in said passivation film by using a fourth mask~~; and

(e) depositing a reflective metal over the rough surface of said interlayer insulating film to form ~~by using a fifth mask~~ a reflection electrode [[being]] extended and electrically connected to said source ~~wiring~~ electrode through the first and second openings ~~for the transistor in said passivation film and said interlayer insulating film~~.

2. (currently amended) A process for producing a reflection type liquid crystal display device, comprising the steps of

(a) depositing a low resistance metal layer on an insulating substrate, and using a first mask to pattern the metal layer to form [[a]] source/drain ~~wiring by using a first mask~~ electrodes;

(b) depositing a silicon layer, gate insulating film and gate electrode layer on said insulating substrate having said

source/drain ~~wiring formed~~ electrodes in this order and using a second mask to pattern the silicon layer, the gate insulating film and the gate electrode layer to form a thin film transistor region and a gate electrode ~~wiring by using a second mask~~;

(c) depositing a passivation film and an interlayer insulating film on said insulating substrate having said source/drain ~~wiring~~ electrodes, said thin film transistor region and said gate ~~wiring formed~~ electrode and using a third mask to form [[an]] a first opening ~~for the transistor~~ through said interlayer insulating film, in a predetermined position on said source electrode ~~wiring by using a third mask~~;

(d) forming [[an]] a second opening ~~for the transistor~~ through said passivation film in a position corresponding to the first opening ~~for the transistor~~ in said interlayer insulating film by using said interlayer insulating film as a mask;

(e) depositing a reflective metal over ~~the rough surface of~~ said interlayer insulating film to form ~~by using a fifth mask~~ a reflection electrode [[being]] that is extended through the respective first and second openings ~~for the transistor~~ in said passivation film and said interlayer insulating film and electrically connected to said source electrode ~~wiring~~.

3. (currently amended) The process as defined in claim 1 wherein the formation of the rough surface of said interlayer

insulating film and the second opening ~~for the transistor~~ is conducted by halftone exposure or two-times exposure.

4. (currently amended) The process as defined in claim 3, wherein the formation of the rough surface of said interlayer insulating film and the second opening ~~for the transistor~~ is conducted by using ~~an exposure~~ the fourth mask having controlled transmissivity ~~being controlled~~.

5. (currently amended) ~~A process as defined in claim 1 further comprising the steps of:~~

A process for producing a reflection type liquid crystal display device, comprising the steps of:

(a) depositing a low resistance metal layer on an insulating substrate, and using a first mask to pattern the metal layer to form source/drain electrodes;

(b) depositing a silicon layer, gate insulating film and gate electrode layer on said insulating substrate having said source/drain electrodes formed thereon in this order, and using a second mask to pattern the silicon layer, the gate insulating film and the gate electrode layer to form a thin film transistor region and a gate electrode;

(c) depositing a passivation film on said insulating substrate having said source/drain electrodes, said thin film

transistor region and said gate electrode formed thereon, and using a third mask to form a first opening through said passivation film to said source electrode;

(d) depositing an interlayer insulating film on said passivation film, forming a rough surface of said interlayer insulating film, and using a fourth mask to form a second opening through said interlayer insulating film at a position corresponding to the first opening;

(e) depositing a reflective metal over the rough surface of said interlayer insulating film to form a reflection electrode extended and electrically connected to said source electrode through the first and second openings

(f) forming a capacitor electrode when said source/drain ~~wirings~~ electrodes are formed; and

~~forming said gate wiring on said insulating substrate having said capacitor electrode formed when forming said thin film transistor region and said gate wiring are formed;~~

(g) forming [[an]] a third opening for a storage capacitor ~~penetrating~~ through said interlayer insulating film and said passivation film in a position on said capacitor electrode when the first and second openings ~~for the transistor is~~ are formed, ~~through said interlayer insulating film and said passivation film; and~~

~~forming~~ wherein said reflection electrode ~~extending~~ extends through the third opening ~~openings for the storage capacitance in said passivation film and in said interlayer insulating film and being~~ and is electrically connected to said capacitor electrode ~~when said reflection electrode is formed~~.

6. (cancelled).

7. (original) The process as defined in claim 1 further comprising the step of heat treating at least the rough surface of said interlayer insulating film before depositing said reflective metal and after forming the rough surface of said interlayer insulating film.

8. (currently amended) The process as defined in claim 1 further comprising the step of treating at least said source/drain ~~wiring~~ electrodes with [[PH_{33}]] PH_3 after said source/drain ~~wiring has been~~ electrodes are formed and prior to successive deposition of said silicon layer, gate insulating film and gate electrode layer.

9. - 16. (cancelled).